

AN/C-BUS/2 December 2002

Introduction

This document is meant to serve as a definition and introduction to the C-BUS microcontroller interface. Most new products from CML use C-BUS, so a basic understanding of this interface will help any design engineer with their evaluation and implementation of CML devices.

Timing parameters with wide applicability to CML products are discussed in this application note. For detailed information concerning specific signal timing requirements, please refer to the respective CML device data bulletin. For any questions on this material or on any CML product, please contact CML at www.cmlmicro.com.

C-BUS Overview

C-BUS is the name given to the synchronous serial microcontroller (μ C) interface developed by CML Microcircuits. C-BUS is compatible with most common serial μ C interfaces and may easily be implemented with general purpose μ C I/O pins controlled by a simple software routine if needed.

Most C-BUS devices transfer data in eight-bit bursts across the interface. Data transfers requiring more than eight bits are completed using multiple eight-bit bursts. A complete data transfer, also called a *transaction*, which comprises of all actions that occur between the active (falling edge) and inactive (rising edge) states of the "Chip Select" pin.

Example C-BUS timing diagrams are included at the end of this document.

Note: The references to active low C-BUS pins will followed with an 'N' for negate. e.g. Chip Select = CSN (some documents may refer to this as /CS or bar CS)

Hardware Description

Chip Select (CSN)

The Chip Select pin (CSN) is an active low signal that initiates, completes, or aborts all C-BUS sequences.

CSN is taken low to start a transaction and should not be taken high until the transaction is completed. If CSN is taken high during a transaction, that transaction is aborted. The CSN signal must be held low during data transfers and kept high between transfers.

Only one register can be written to or read from during a single C-BUS transaction. Multiple register manipulations cannot be performed during a single C-BUS transaction (e.g. taking CSN low, writing to multiple registers, reading from multiple registers, and then taking CSN back high will cause erroneous operation).

Once a C-BUS transaction is complete, the CSN signal must be taken to a high logic level and kept at a high logic level for a prescribed amount of time before the next transaction can begin. This parameter is typically referred to as “ t_{CSOFF} ” (CSN-High Time Between Transactions) in CML product literature.

Serial Clock (SCLK)

The Serial Clock (SCLK) signal is the timing source that controls communications with the CML device. All C-BUS commands and data transfers are synchronized to this clock signal.

Data is transferred to and from the CML device on the rising edge of the Serial Clock signal.

The SCLK speed can usually be any frequency of clock speed within the minimum & maximum as quoted in the device data sheet.

C-BUS data must be stable for a minimum amount of time before the rising edge of the Serial Clock signal; this amount of time is typically referred to as “ t_{CDS} ” (Command Data Set-Up Time). Similarly, there is a minimum time requirement for which the data signal must be stable after the Serial Clock signal rising edge; this parameter is frequently referred to as “ t_{CDH} ” (Command Data Hold Time) in CML product literature. The Serial Clock signal can be asymmetric (i.e. non-50% duty cycle).

There is a minimum amount of time required between the falling edge of the CSN signal and the first Serial Clock rising edge used to strobe in data. This parameter is typically referred to as “ t_{CSE} ” (CSN Enable to Clock High Time). The minimum period between the last rising Serial Clock edge used to strobe in data and the rising edge of the CSN signal is labeled “ t_{CSH} ” (Last Clock High to CSN High Time) in the CML literature.

Command Data

The Command Data line is used to transfer register addresses and device configuration data to the selected CML device.

The first byte that must be transmitted to the CML device in a C-BUS transaction is called the “Address/Command” (A/C) byte. The A/C byte, transmitted on the

Command Data line, specifies the CML device and register to be operated on. An A/C byte can then be followed by one of the following:

- 1) Data bytes from the μC (via the Command Data line) to configure the device register for specific operation.
- 2) Data bytes from the CML device (via the Reply Data line), such as status register contents.

In general, all bytes are transmitted most significant bit (msb) first. For multiple byte C-BUS transactions there is usually a short time period between the bytes transferred in the transaction; this time period is typically referred to as “ t_{NEXT} ” (Inter-Byte Time).

Command Data must be valid on the low-to-high transition of the Serial Clock. Consequently, it may be convenient to configure the software such that the Command Data is changed on the high-to-low transition of the Serial Clock.

The “General Reset” command is a single byte C-BUS transaction; there is no data associated with the command.

Reply Data

The Reply Data line is used to transfer requested data from the CML device to the host μC .

Reply Data is only available if a command (request) is first sent to the CML device on the Command Data line. There is usually a short time period between the transferred bytes in multiple byte C-BUS transactions; this time period is typically referred to as “ t_{NEXT} ” (Inter-Byte Time).

Data on the Reply Data line is valid when the Serial Clock signal is high, and it may be read into the μC on the Serial Clock low-to-high transition.

Interrupt Request (IRQN)

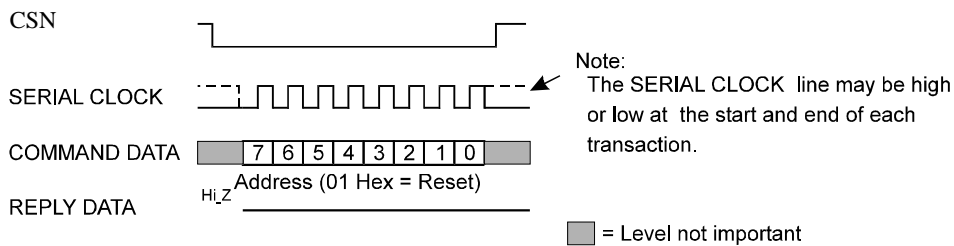
The Interrupt Request line is an active low signal that indicates when the CML device is in need of servicing by the μC . The IRQN line is typically connected to V_{DD} via a pull-up resistor; refer to the respective CML device data bulletin for recommended pull-up resistor values.

Many CML devices allow the “masking” of interrupts by the selection of appropriate register bits; please refer to the respective CML device data bulletin for more information.

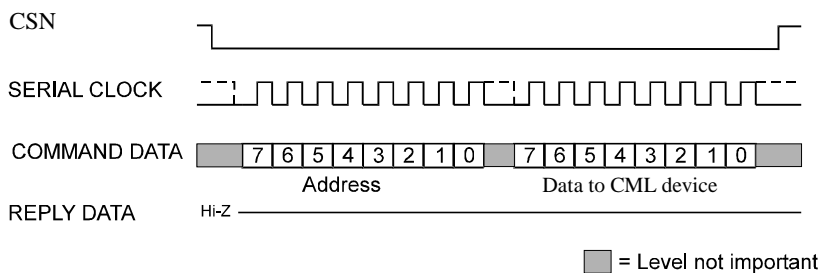
Examples Of C-Bus Transactions

The examples below describe five transactions for C-BUS and one transaction for the CMX264. Note that the events between the low and high states of CSN form one complete transaction.

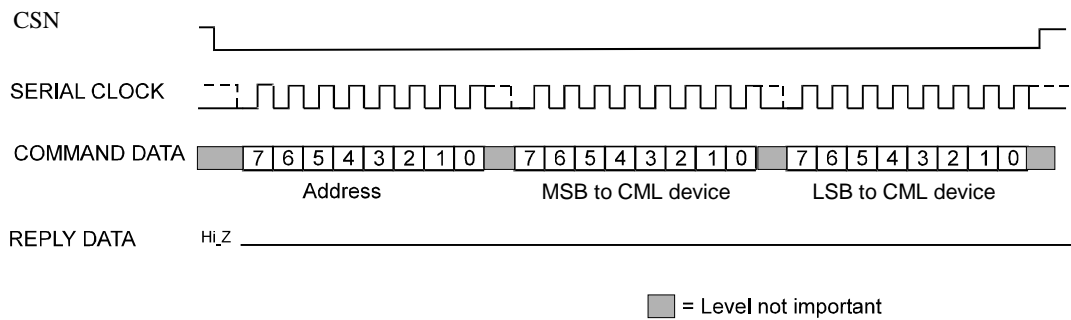
1. A single byte C-BUS transfer (e.g. "General Reset" command):
 - a. Take CSN low.
 - b. Send Address/Command byte containing General Reset command on Command Data line.
 - c. Take CSN high.



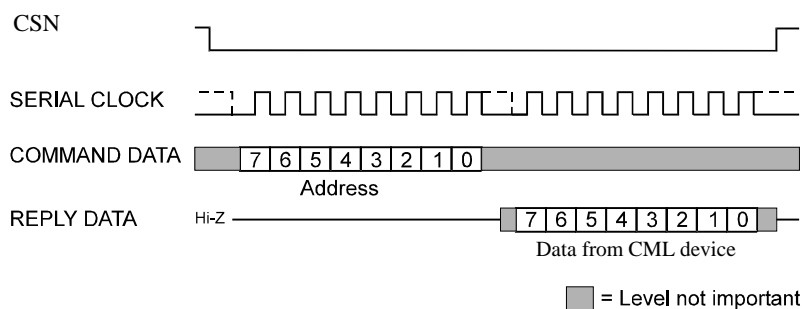
2. A two-byte C-BUS transfer to the CML device (e.g. to set up a control register):
 - a. Take CSN low.
 - b. Send Address/Command byte (containing desired register) on Command Data line.
 - c. Send data byte (register configuration byte) on Command Data line.
 - d. Take CSN high.



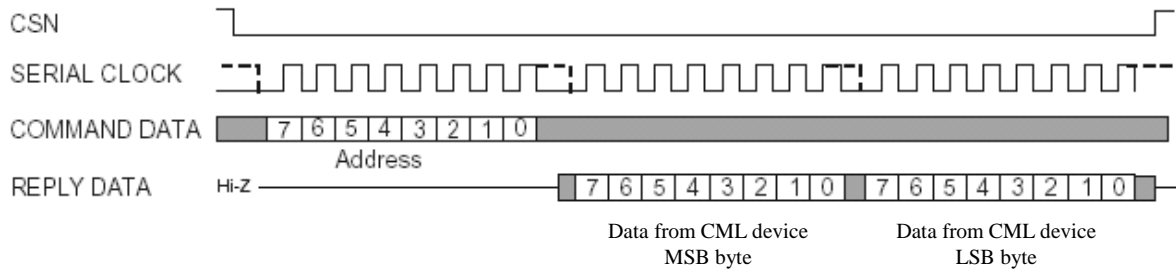
3. A three-byte C-BUS transfer to the CML device (e.g. to set up a data word register):
 - a. Take CSN low.
 - b. Send Address/Command byte (containing desired register).
 - c. Send first data byte (half of data word).
 - d. Send second data byte (remainder of data word).
 - e. Take CSN high.



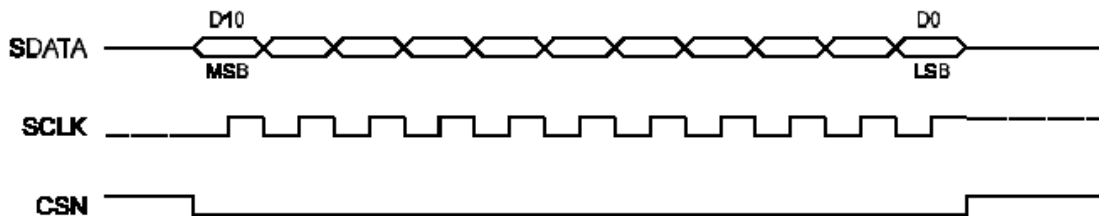
4. A two-byte C-BUS transfer to and from the CML device (e.g. request for status):
 - a. Take CSN low.
 - b. Send Address / Command byte (containing desired register to be read).
 - c. Read Reply Data byte (register contents).
 - d. Take CSN high.



5. A three-byte C-BUS transfer to and from the CML device (e.g. request for status):
 - a. Take CSN low.
 - b. Send Address / Command byte (containing desired register to be read).
 - c. Read Reply Data bytes (register contents).
 - d. Take CSN high.



6. A single 11 bit write transaction on the CMX264:
 - a. Take CSN low.
 - b. Send Address / Command byte.
 - c. Take CSN high.



Only one register (write-only) is available on the CMX264; no other transactions are valid. The CMX264 only reads the last 11 bits of any transfer (completed when CSN goes high). Thus, it may be convenient to write all sixteen bits (normal word or two byte length) available. The additional leading bits will be ignored.

CONCLUSION

The C-BUS microcontroller interface is a simple five-wire interface developed by CML Microcircuits. The C-BUS interface is compatible with common μ C interfaces and can easily be implemented with general purpose I/O pins and a simple software loop if needed.




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For FAQs see: <http://www.cmlmicro.com/products/faqs/index.htm>

For a full data sheet listing see: <http://www.cmlmicro.com/products/datasheets/download.htm>

For detailed application notes: <http://www.cmlmicro.com/products/applications/index.htm>

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